4.5V-100V Vin, 1A, Constant On-Time Synchronous BUCK Converter

- Wide Input Range: 4.5V-100V
- 1A Continuous Output Current
- Integrated 530mÝ High-Side and 220mq Low-Side Power MOSFETs
- 150

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Market

Revision 1.1: Update DEVICE ORDER INFORMATION.

SCT2A21STERenU					

BST	7	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
SW	8	Regulator switching output. Connect SW to an external power inductor
Thermal Pad	9	Heat dissipation path of die and also is GND PIN. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

Over operating free-air temperature range unless otherwise noted

V_{IN}	Input voltage range	4.5	100	V
V_{CC}	External V_{CC} bias voltage	7.5		

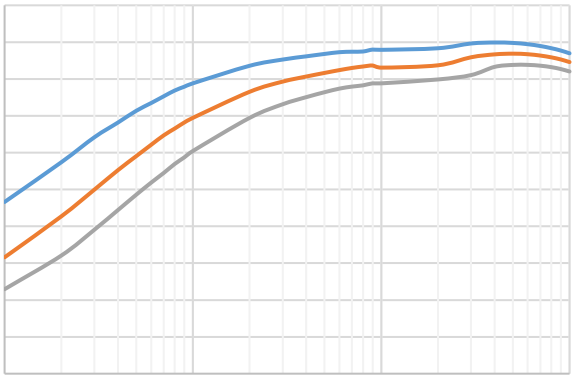

Figure 2. Efficiency, Fsw=300k, Vout=5V

Figure 3. Efficiency, Fsw=300k, Vout=12V

Figure 4. Vin Active Current vs Input Voltage, Vout=12V

Figure 5. I_Q vs Input Voltage

Figure 6. Line Regulation, Vout=12V, Iload=0.5A

Figure 7. Fsw VS Vin, Vout=12V, Ron=400K

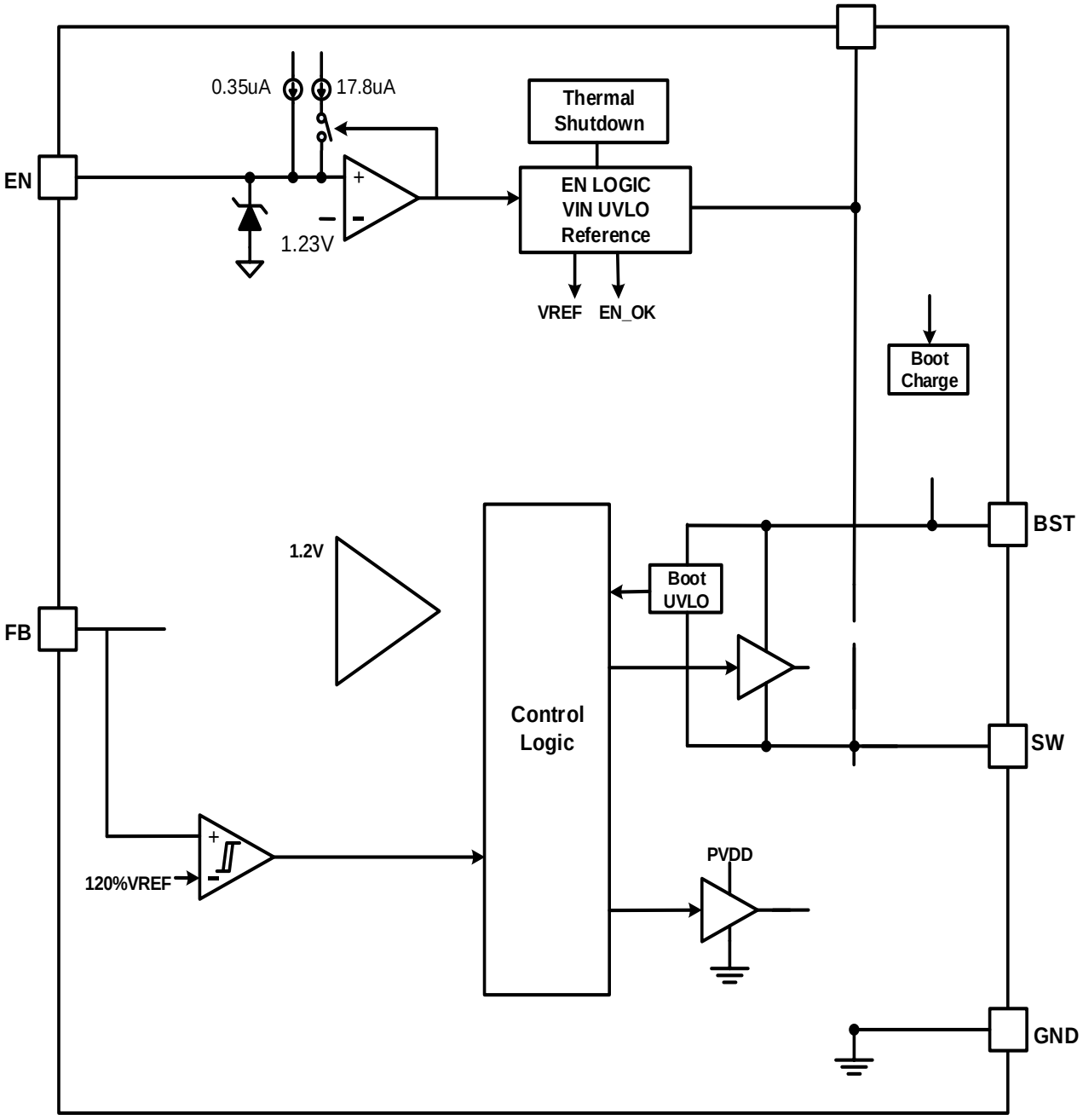

Figure 8. Functional Block Diagram

The SCT2A21 is a 4.5V-100V input, 1A output, synchronous buck converter with built-in 530mq high-side and 220mq low-side power MOSFETs. It implements constant on time control to regulate output voltage, providing excellent line and load transient response.

The device operates in Pulse Frequency Modulation (PFM) mode at light loading to provides high light load efficiency. The quiescentþ ⁎ l M

SCT2A21 converter output rail if the regulation voltage. When the VCC pin of the SCT2A21 is raised above the regulation voltage (7.3V typical), the internal regulator is disabled and the power dissipation in the IC is reduced.

The SCT2A21 is enabled when the VIN pin voltage rises about 4.1V and the EN pin voltage exceeds the enable threshold of 1.23V. The device is disabled when the VIN pin voltage falls below 3.88V or when the EN pin voltage is below 1.22V. An internal 0.35uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R3 and R4) shown in Figure 10 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 6 and Equation 7 respectively.

$$\text{سي} \quad \frac{3 \text{ طى } 4}{4} \qquad (6)$$

$$\text{سي } 2 \quad 3 \qquad (7)$$

Where

VIN_rise: Vin rise threshold to enable the device

VIN_hys: Vin hysteresis threshold

I_1=0.35uA: neglect in calculation

I_2=17.8uA

V_{EN}=1.23V, assume VEN_r = VEN_f =1.23V

The SCT2A21 implements the Over-Voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP

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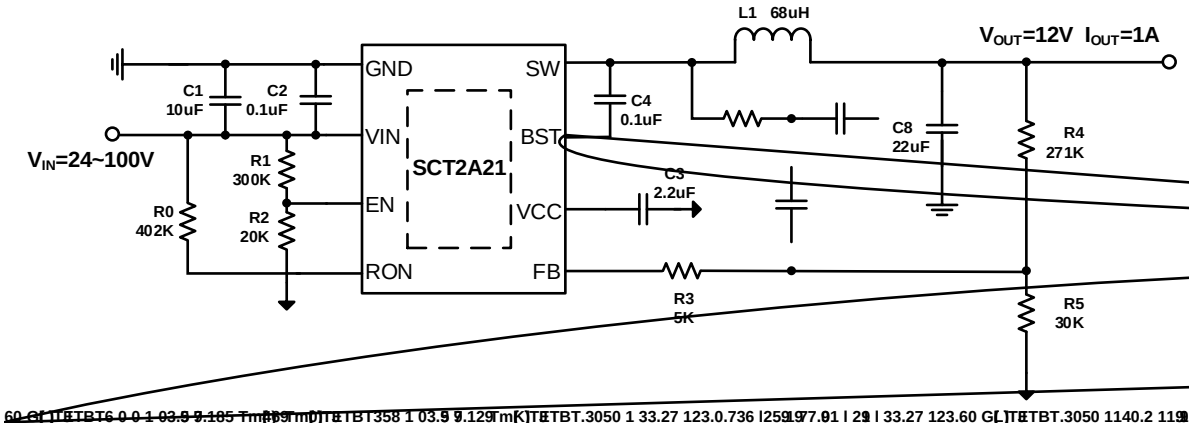
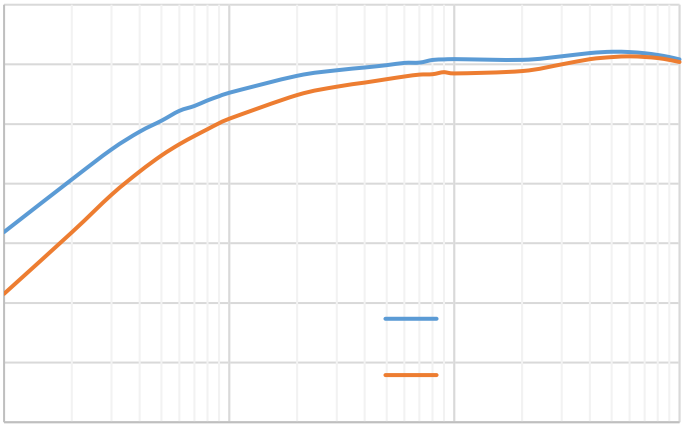


Input Voltage	48V Normal 24V to 100V
Output Voltage	12V
Maximum Output Current	1A
Switching Frequency	300 KHz
Output voltage ripple (peak to peak)	30mV
Transient Response 0.1A to 0.9A load step	æVout = 210mV



The output voltage is set by an external resistor divider R4 and R5 in typical application schematic. Recommended R5 resistance is 30Kq . Use equation 9 to calculate R4.

$$R4 = R5 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (9)$$

where:

- V_{REF} is the feedback reference voltage of 1.2V

Table 1. R_1, R_2Value for Common Output Voltage (Room Temperature)

5 V	95 Kq	30 Kq
12V	271 Kq	30 Kq
24V	576 Kq	30 Kq

An external voltage divider network of R_3 from the input to ER Ỳ ex frqe$ M

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 13 to calculate the inductance value.

$$\text{سي إآؤ} \frac{\text{ااإ}}{\text{بئ ذقجـ ااإ}} \quad 1 \text{ طي} \frac{\text{ااإ}}{\text{ذقجـ إآ}} \tag{13}$$

Where

- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 14 and equation 15.

$$\text{ؤئ}_{\circ}\text{ـ أ سي ااإ طى} \frac{\text{ؤئ}}{2} \tag{14}$$

$$\text{ؤئ}^{2} \quad \text{ااإ}^{2} \text{ طى} \frac{1}{12} \quad \text{ؤ ئ ؤ سي شمم} \tag{15}$$

Where

- I_{LPEAK} is the inductor peak current
-

$$I_{CINRMS} \text{ سي } 0.5 \quad I_{OUT} \tag{17}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 18 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} \text{ سي } \frac{I_{OUT}}{f_{SW} \quad C_{IN}} \quad \frac{V_{OUT}}{V_{IN}} \quad 1 \text{ ط} \frac{V_{OUT}}{V_{IN}} \tag{18}$$

For this example, one 10εF, X7R ceramic capacitors rated for 100 V in parallel are used. And a 0.1 εF for high-frequency filtering capacitor is placed as close as possible to the device pins.

A 0.1εF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X7R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 19 desired.

$$\Delta V_{OUT} \text{ سي } \frac{\text{ا ا إ} \quad \text{آ إ ط} \quad \text{ا ا إ}}{8 \quad \text{ئ ت}^{2} \quad \text{ا ا ا} \quad \text{آ ا}} \tag{19}$$

Where

- qV$_{OUT}$is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- $V_{IN}$is the input voltage

Due to capacitorôs degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, one 22εF ceramic output capacitors work for most applications.

Table 2 and Table 3 lists typical values of external components for some standard output voltages.

Vin=48V, Vout=12V, Fsw=300k, unless otherwise noted

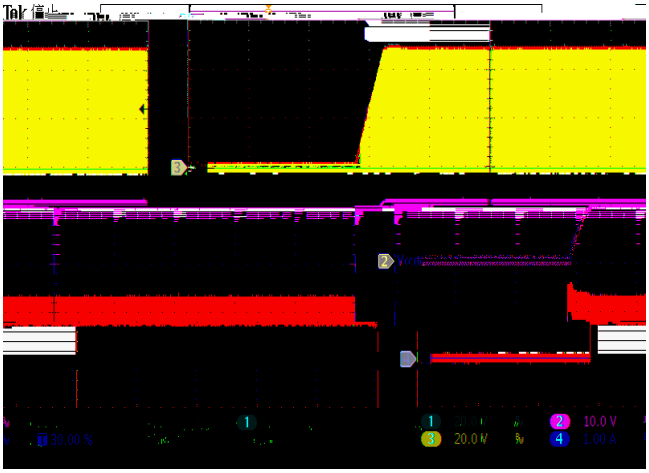


Figure 13. Power up (Iload=1A)

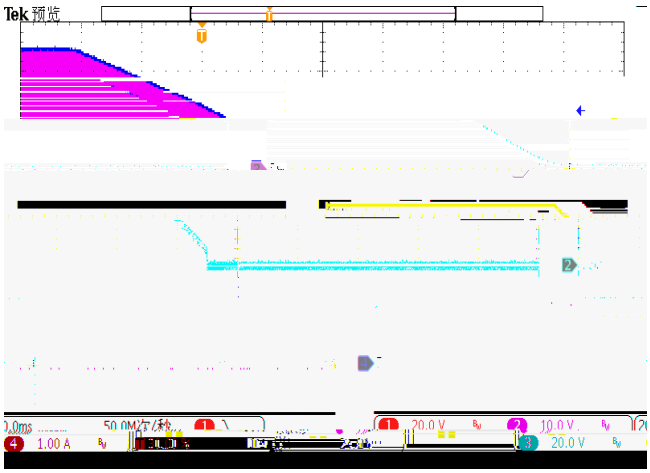


Figure 14. Power down (Iload=1A)

Figure 15. Enable toggle (Iload=0.1A)

Figure 16. Enable toggle (Iload=1A)

Figure 17. Output Hard Short

Figure 18. Output Hard Short Release

Vin=48V, Vout=12V, Fsw=300k, unless otherwise noted

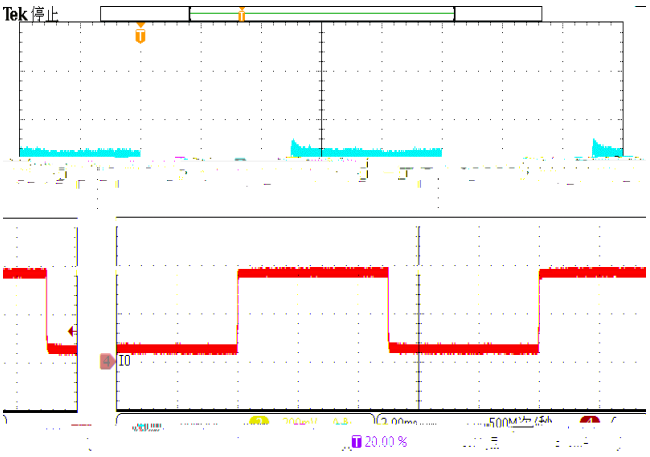


Figure 19. Load Transient (0.1A to 0.9A, 1.6A/us)

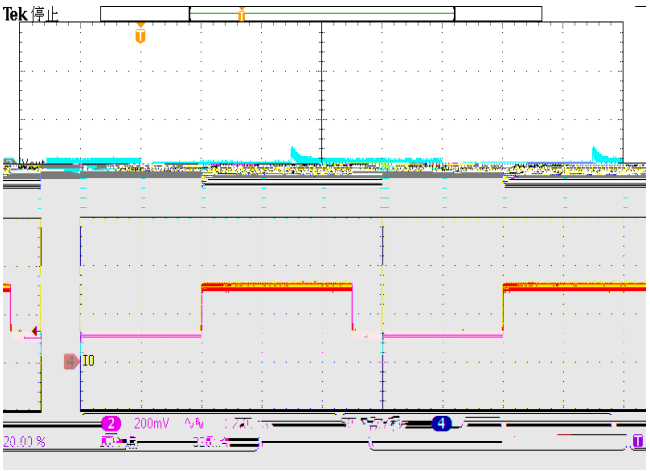


Figure 20. Load Transient (0.25A to 0.75A, 1.6A/us)

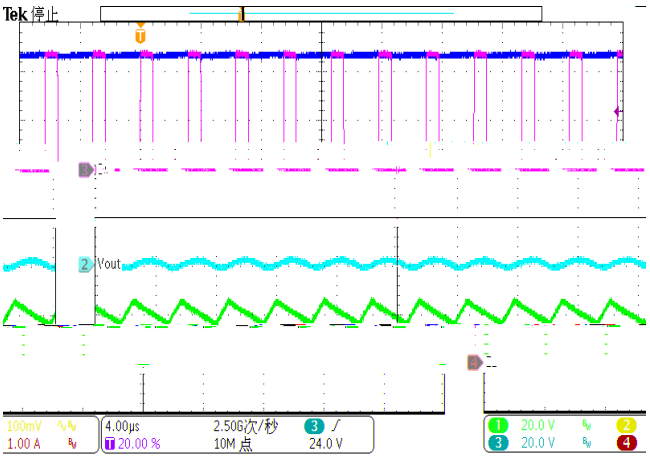


Figure 21. Output Ripple (Iload=1A)

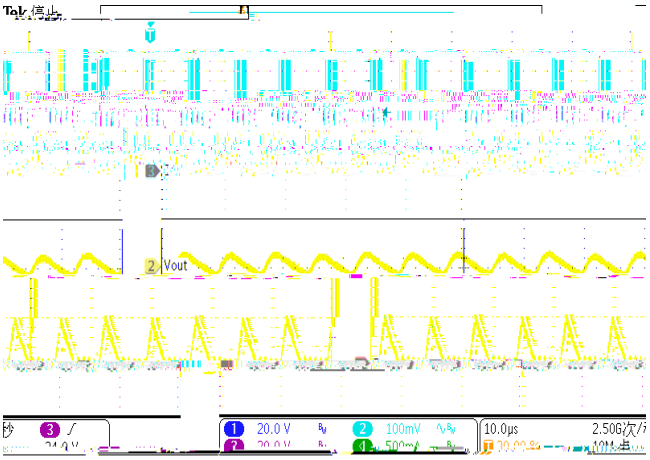


Figure 22. Output Ripple (Iload=0.1A)

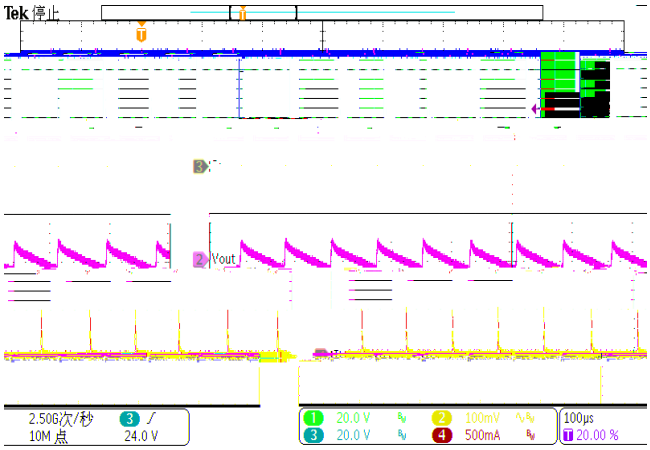


Figure 23. Output Ripple (Iload=0.01A)

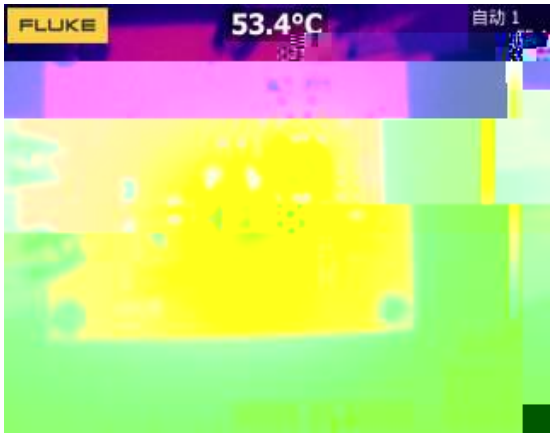


Figure 24. Thermal, 48VIN, 12Vout, 1A

Proper PCB layout is a critical for SCT2A21ꞌs stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.

2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.

3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.

4. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be

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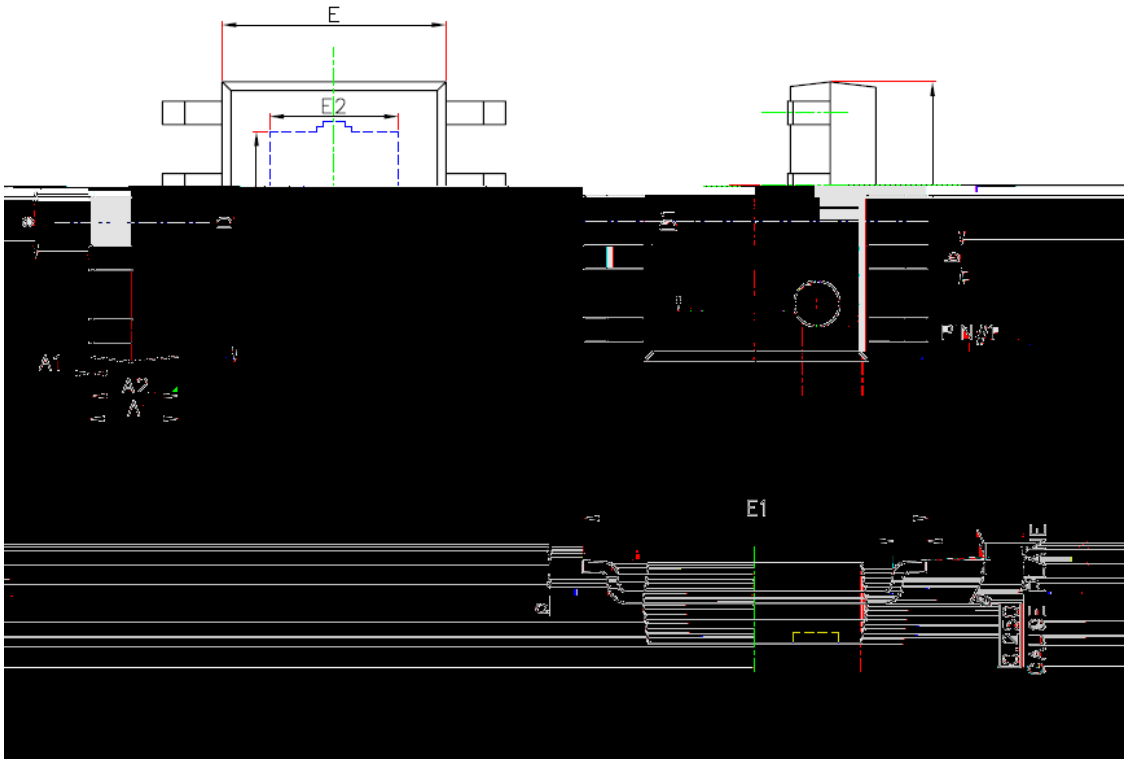

ESOP8(95x130) Package Outline Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0Á	8Á	0Á	8Á

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.