15W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter

- VIN Input Voltage Range: 4.2V-20V
- PVIN Input Voltage Range: 1V-20V
- Up to 15W Power Transfer
- Integrated Full-Bridge Power Stage with 17.5-m Rdson of Power MOSFETs
- Integrated 5V-100mA LDO
- Optimized for EMI Reduction
- Build

5V

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
Revision 1.0: Production
Revision 1.1: Update EC
Revision 1.2: Update DEVICE ORDER INFORMATION

ORDERABLE DEVICE

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63142 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63142. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

V_{PVIN1}=V_{PVIN2}=12V, VDD=5V, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT

V_{ISNS2}	Voltage with 1A input current	I_{PVIN}=1A, Tj=25	1.568	1.6	1.632	V
Protection						
T_{SD}	Thermal shutdown threshold	T_J rising		155		°C

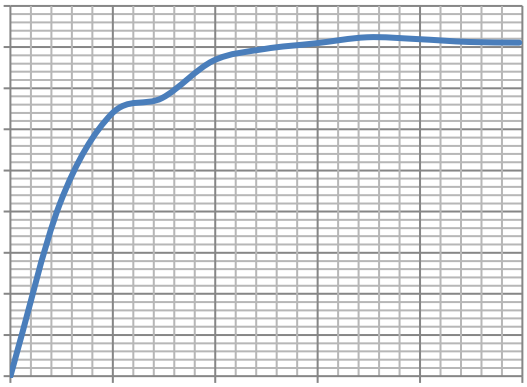


Figure 2. Transfer Efficiency with 5W RX@ Vout=5V

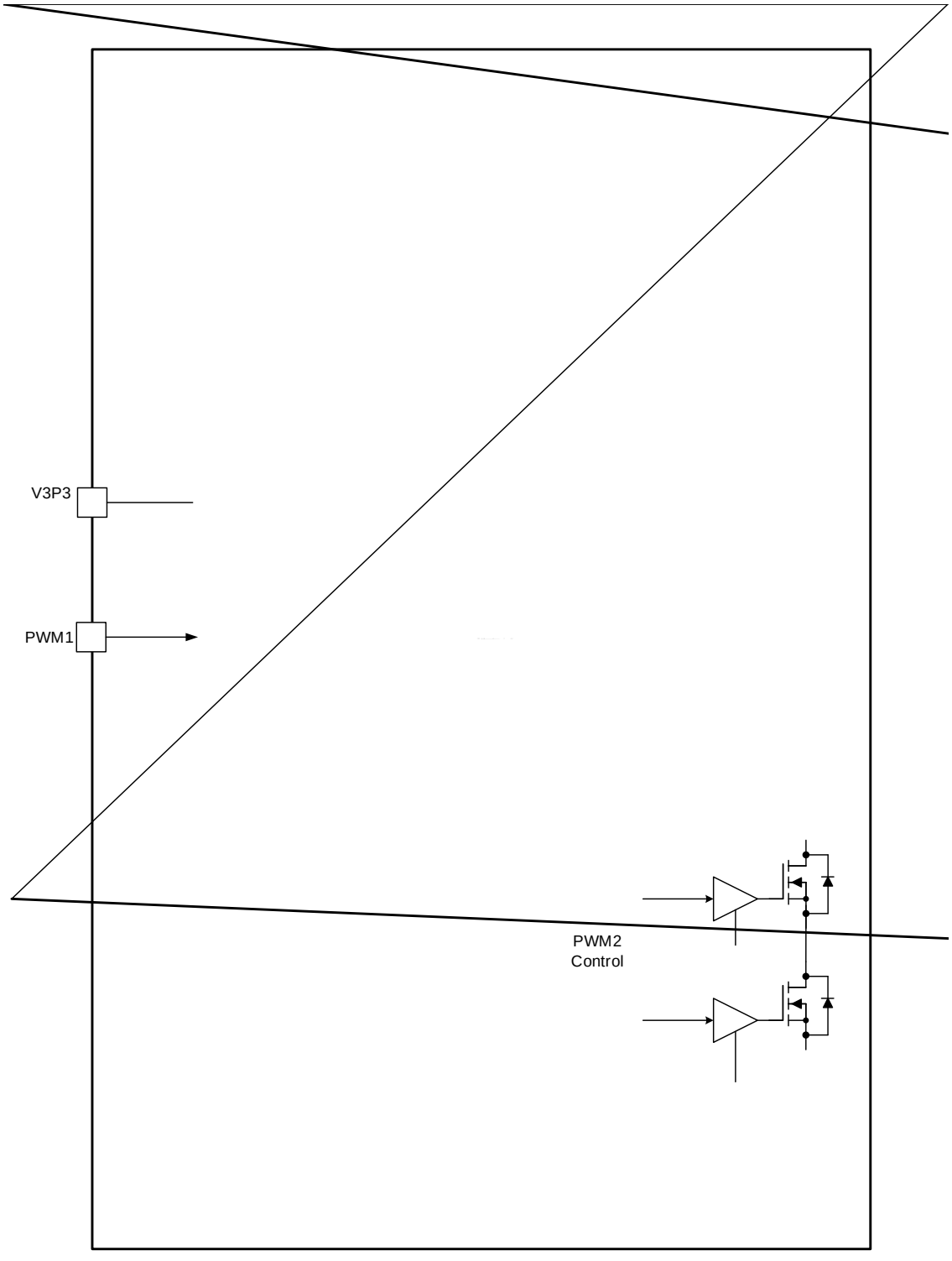
Figure 3. Transfer Efficiency with 10W RX@ Vout=9V

Figure 4. Transfer Efficiency with 15W RX@ Vout=12V

Figure 5. 5V LDO Iout vs Vout

Figure 6. 3.3V LDO Iout vs Vout

Figure 7. Current Sense Output Voltage vs Iin



V

Figure 8. Functional Block Diagram

Overview

The SCT63142 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V output LDO as power supply for external transmitter controller, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, lossless current sensing with ±2% accuracy, 3.3V output LDO for powering MCU.

The SCT63142 has three power input pins. VIN is connected to the power FETs of 5V LDO. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conducts high currents for power transfer.

VIN and PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for VIN is from 4.2V to 20V. An Under-Voltage Lockout(UVLO) circuit monitors the voltage of VIN pin and disable the IC operation when VIN voltage falls below the UVLO threshold of 3.08V typically. The maximum operating voltage for PVIN is up to 20V while the minimum voltage accepted can be down to 1V. Another UVLO circuit also supervise the VDD voltage which is the power supply for gate drivers of full bridge MOSFETs. Full bridge will work when VDD UVLO release.

Two independent PWM signals control two separate half bridge MOSFETs with internal adaptive non-overlap circuitry to prevent the shoot-through of MOSFETs in each bridge. PWM logics are compatible for both 3.3V and 5V IOs so the SCT63142 can accept PWM signal from the controller with using either 3.3V or 5V power supply.

The full bridge of power MOSFETs includes proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. This allows the user to reduce the system cost and design effort for EMI reduction.

The SCT63142 full protection features include VIN and VDD under-voltage lockout, over current protection with cycle-by-cycle current limit and hiccup mode, output hard short protection for 4-MOSFETs full bridge, current limit and current fold back at hard short for two LDOs and whole chip thermal shutdown protection.

Enable and Start up Sequence

When the VIN pin voltage rises above 3.6V and the EN pin voltage exceeds the enable threshold of 1.18V, the 5V output LDO enables at once. And the device disables when the VIN pin voltage falls below 3.2V or when the EN pin voltage is below 1.1V. VDD ramp up after 5V LDO works, and also the V3V. Once VDD rise up to 3.8V and V3V is higher than 3V, 4-MOSFETs full bridge allows PWM signal to control for switching. PWM input cannot control full bridge of MOSFETs if VDD drop to 3.36V or V3V drop to 2.7V.

An internal 1.5uA pull up current source to EN pin allows the device

3.3V LDO

The SCT63142 has an integrated low-dropout voltage regulator which powered from VDD and supply regulated 3.3V voltage on V3V pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of MCU directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the V3V pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Q Factor Detection

The SCT63142 integrated a low cost, reliable Q factor detection circuit to assure foreign objects detection before the selection phase. It generates a small pulse to detect any foreign object on the transmitter coil, it can detect metal on the transmitter coil easily.

After chip enable, apply a low voltage level pulse to EN pin can trigger the Q factor detection feature. The pulse width should be longer than 50us but less than 200us. SW1 will be preset to 2V for 4.7ms and then pull low to ground and this apply power to LC resonant loop and Vcoil will appear damping oscillation after SW1 short to ground. The SCT63142 will generate a pulse on VDMO pin and MCU can capture this pulse to calculate the Q factor by the pulse width as the Equation 4 shows. PWM1 and PWM2 should be low in Q factor detection phase.

Thermal Shutdown

The SCT63142 protects the device from the damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 155C, the thermal sensing circuit stops two LDOs and full bridge of 4-MOSFETs' working. When the junction temperature falls below 120C, then the device restarts.

Typical Application

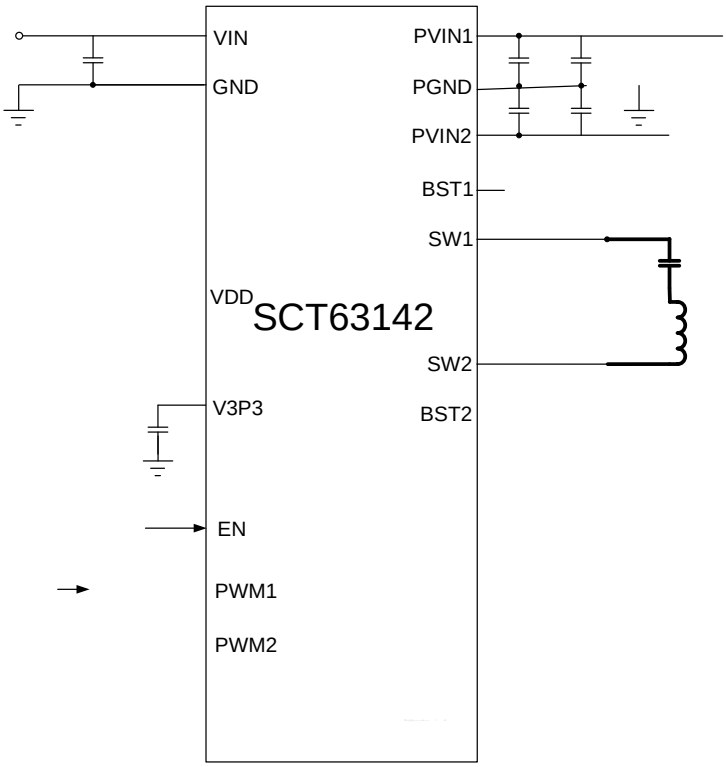


Figure 11. Same Input to VIN and PVIN

Application Waveforms

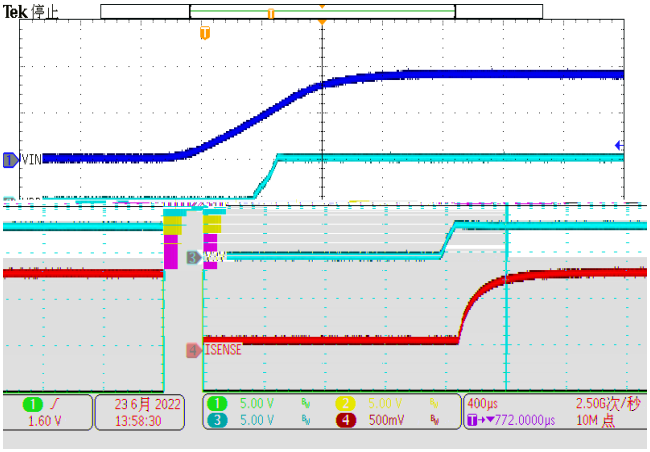


Figure 12. Power Up

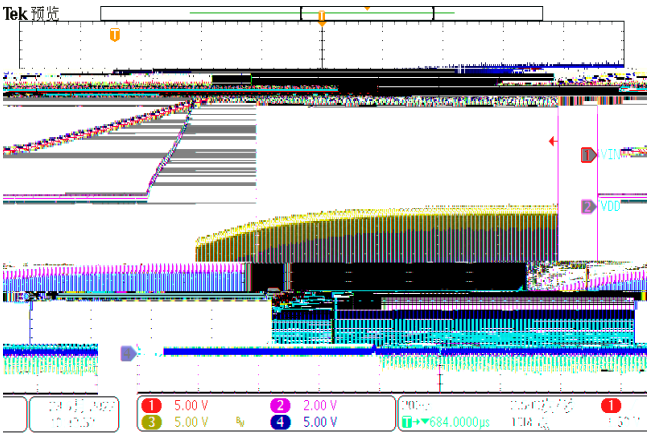


Figure 13. Power Up

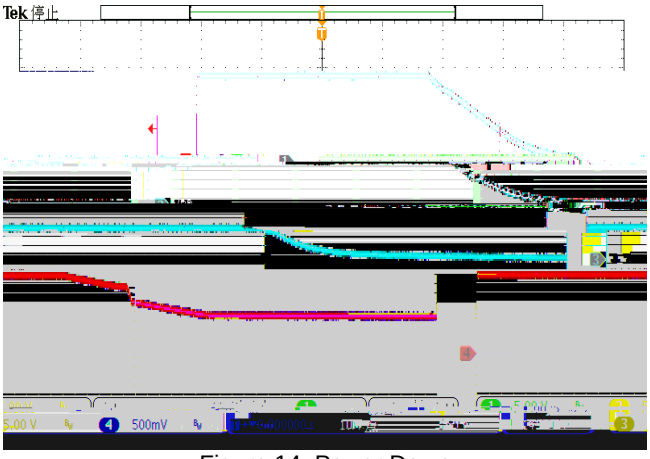


Figure 14. Power Down

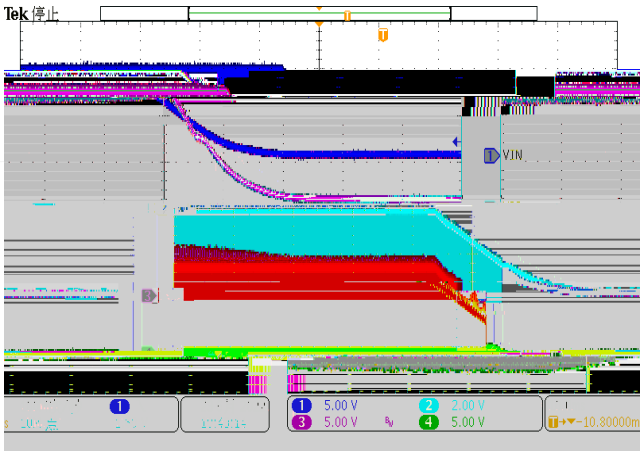


Figure 15. Power Down

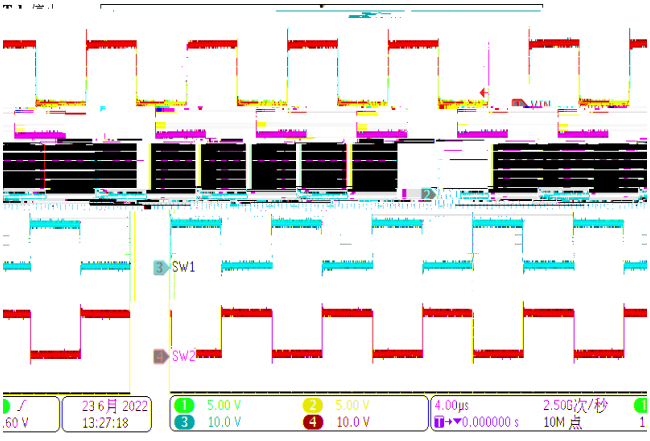


Figure 16. Full bridge @Vin=9V, RX=10W

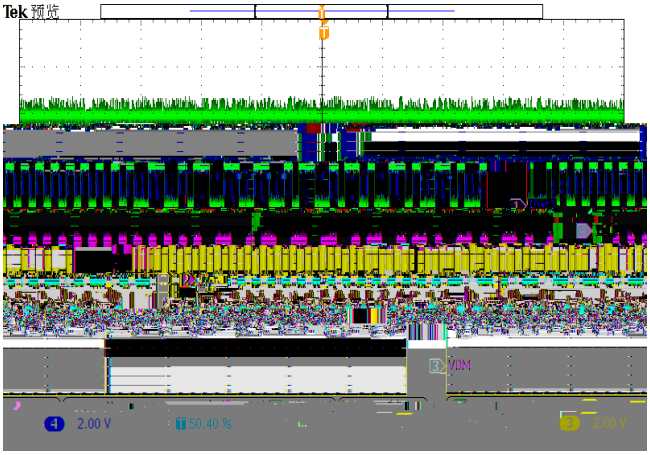


Figure 17. VDMO IDMO Demodulation Output

Layout Guideline

Proper PCB layout is a critical for SCT63142 For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND shoulND soesi PG1sND s24(e(D)-6u)5(s)-n (s)-5(s)-14(ap)(ow)-3(ase (s)-5(s)-)-(

FCQFN-19L (3x3) Package Outline Dimensions

		Symbol	Dimensions in Millimeters		
			Min.	Nom.	Max.
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	3.00 BSC		
	Y	E	3.00 BSC		
LEAD PITCH		e