2.8V-6V Vin 3A Synchronous Step Down Convertor

Revision 0.8: Customer sample.

V_{IN}=5V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.8		6	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising		2.7		V
	Hysteresis			175		mV
I_{SD}	Shutdown current			0		

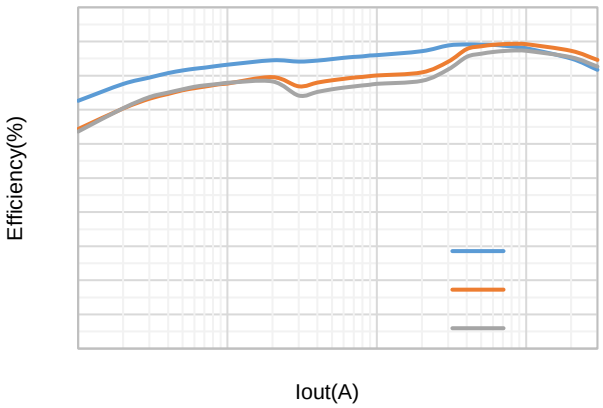

Figure 1. Efficiency vs Load Current, Vout=1.2V

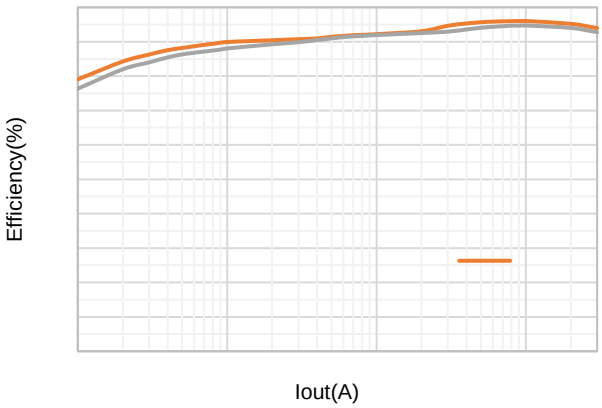

Figure 2. Efficiency vs Load Current, Vout=3.3V

Figure 3. Line Regulation, Io=1.5A

Figure 4. Load Regulation, Vin=5V

Figure 5. V_{FB} vs Temperature

Figure 6. UVLO vs Temperature

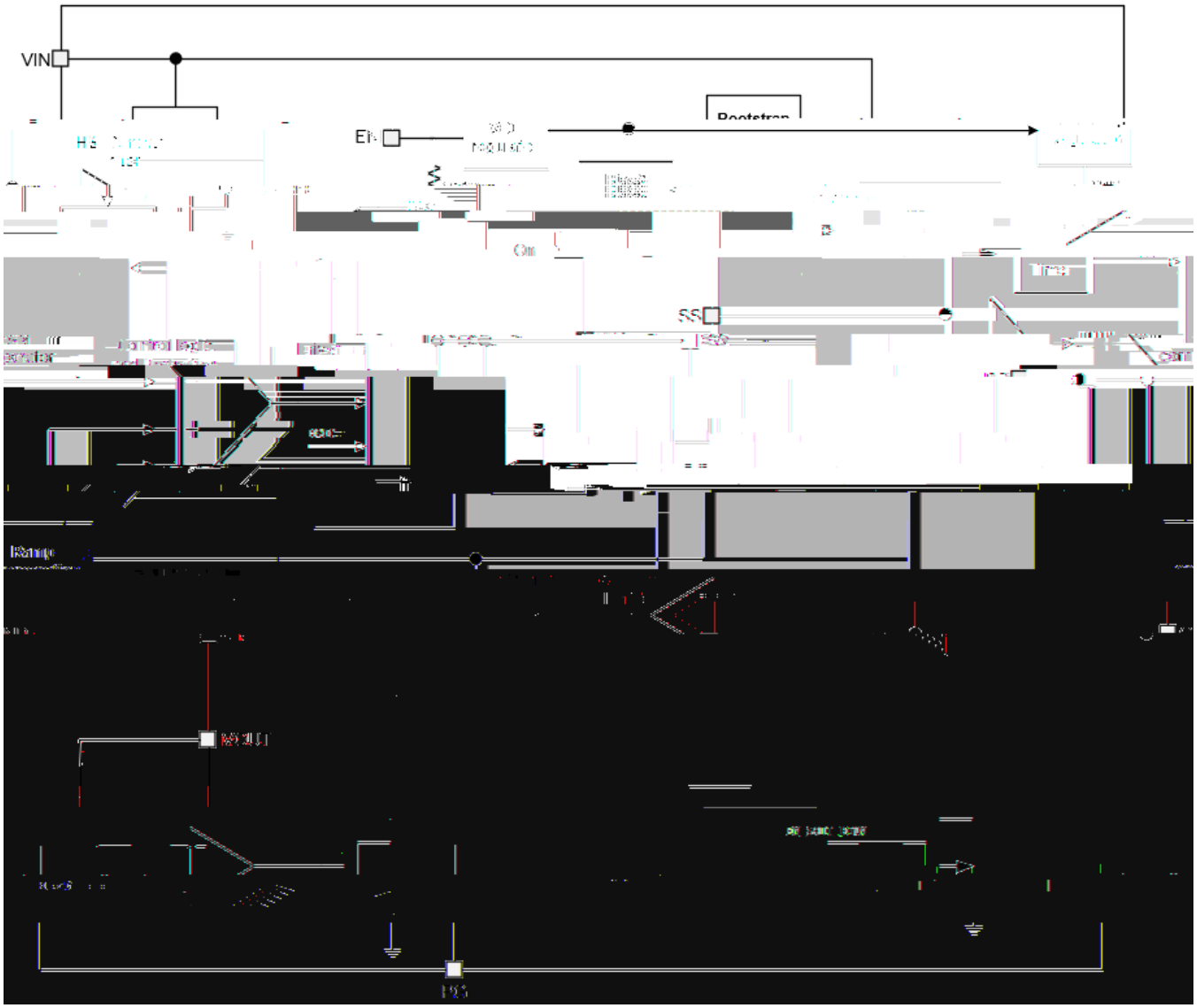

Figure 7. Functional Block Diagram

Overview

The SCT2131Q is a 2.8V-6V input, 3A output, synchronous buck converter with built-in 25m high-side and 20m Rdson low-side power MOSFETs. It implements constant on time control to regulate output voltage, providing excellent line and load transient response, and internal error amplifier integrated improve the line and load regulation.

The switching frequency is fixed 2.1MHz. The SCT2131Q features programmable soft start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The SCT2131Q operates in Pulse Frequency Modulation (PFM) to improve low light load efficiency. The quiescent current is typically 65uA under no load and no switching.

The SCT2131Q full protection features include the input under-voltage lockout, over current protection with

When the device is disabled, the part automatically goes into output discharge mode, and its internal discharge MOSFET in VOUT pin provides a discharge path for the output capacitor.

Output Voltage

The SCT2131Q regulates the internal reference voltage at 0.6V. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 2 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

(2)

Where:

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Soft Start (SS)

The SCT2131Q has an external soft start (SS) pin that ramps up the output voltage at a controlled slew rate to -start time (tss) is determined by the SS capacitor. tss can be calculated with Equation 3:

(3)

Where:

- Css is the ex3( )-o1 0 0 1 263.57 397 reW* nBT/F16 8.521 TP1he ground.

voltage is pulled to GND to indicate an output failure. If VIN and EN are not available, and PG is pulled up by an external power supply, PG will self- -up resistor is used, the voltage on the pin is below 0.4V.

Typical Application

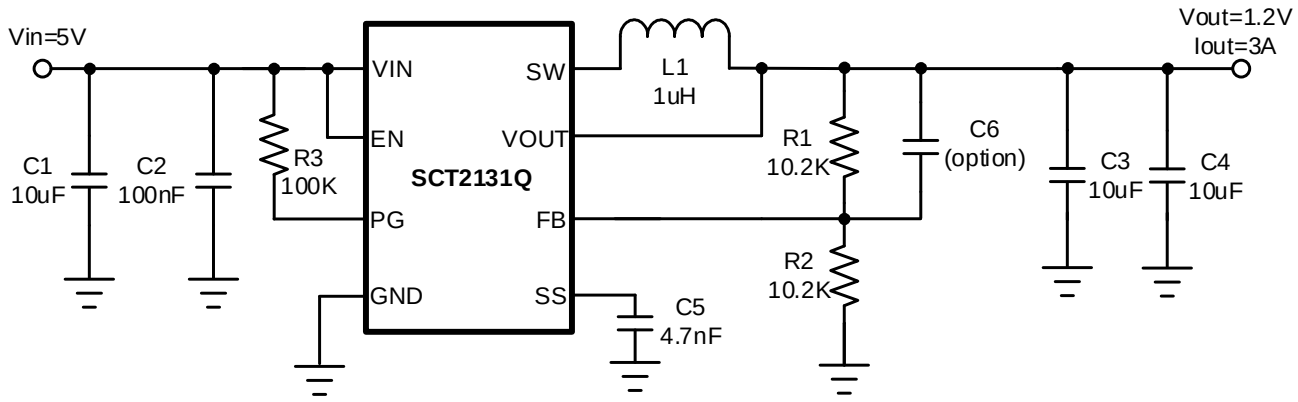

Figure 8. SCT2131Q Design Example, 1.2V Output

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal 2.8V to 6V
Output Voltage	1.2V
Maximum Output Current	3A
Switching Frequency	2.1MHz
Output voltage ripple (peak to peak)	2mV
Transient Response 0.3A to 2.7A load step	Vout =140mV

Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 10.2K . Use Equation 4 to calculate R1.

Application Waveforms

V_{IN}=5V, V_{OUT}=1.2V, unless otherwise noted

Figure 9. Power up (I_{LOAD}=3A)

Figure 10. Power down (I_{LOAD}=3A)

Figure 11. EN toggle (I_{LOAD}=0.1A)

Figure 12. EN toggle (I_{LOAD}=3A)

Figure 13.

Application Waveforms

Figure 15. Load Transient (0.3A-2.7A, 1.6A/us)

Figure 16. Load Transient (0.75A

Layout Guideline

Proper PCB layout is a critical for SCT2131Q . The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing overheat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB groundW* nBT/F21 9.96 Tf 9.onlonl grou-8(p)-57er i eff nn.