

SCT2132Q

Revision 1.0: Release to production.

Revision 1.1: Update DEVICE ORDER INFORMATION and the parameter of $ILIM_{LS}$ and the value of I_Q .

Revision 1.2: Add annotations for T_{sd} , t_{on_min} and t_{off_min}

Over operating free-air temperature range unless otherwise noted

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|-----------|----------------------|-----|-----|------|
| V_{IN} | Input voltage range | 2.8 | 6 | V |
| V_{OUT} | Output voltage range | 0.6 | 5 | V |

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$V_{IN}=5V$, $T_J=-40\text{ }^{\circ}\text{C}\sim 125\text{ }^{\circ}\text{C}$, typical values are tested under $25\text{ }^{\circ}\text{C}$.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--------------------------------|---------------------------------|-----------------------|-----|-----|-----|---------------|
| Power Supply and Output | | | | | | |
| V_{IN} | Operating input voltage | | 2.8 | | 6 | V |
| V_{IN_UVLO} | Input UVLO | V_{IN} rising | | 2.7 | | V |
| | Hysteresis | | | 175 | | mV |
| I_{SD} | Shutdown current | | 0.7 | 3 | | μA |
| I_Q | Quiescent current from V_{IN} | no load, no switching | | 460 | 645 | μA |

V



Figure 1. Efficiency vs Load Current, Vout=1.2V

Figure 2. Efficiency vs Load Current, Vout=1.8V

Figure 3. Line Regulation, Io=1.5A

Figure 4. Load Regulation, Vin=5V

Figure 5. V_{FB} vs Temperature

Figure 6. UVLO vs Temperature

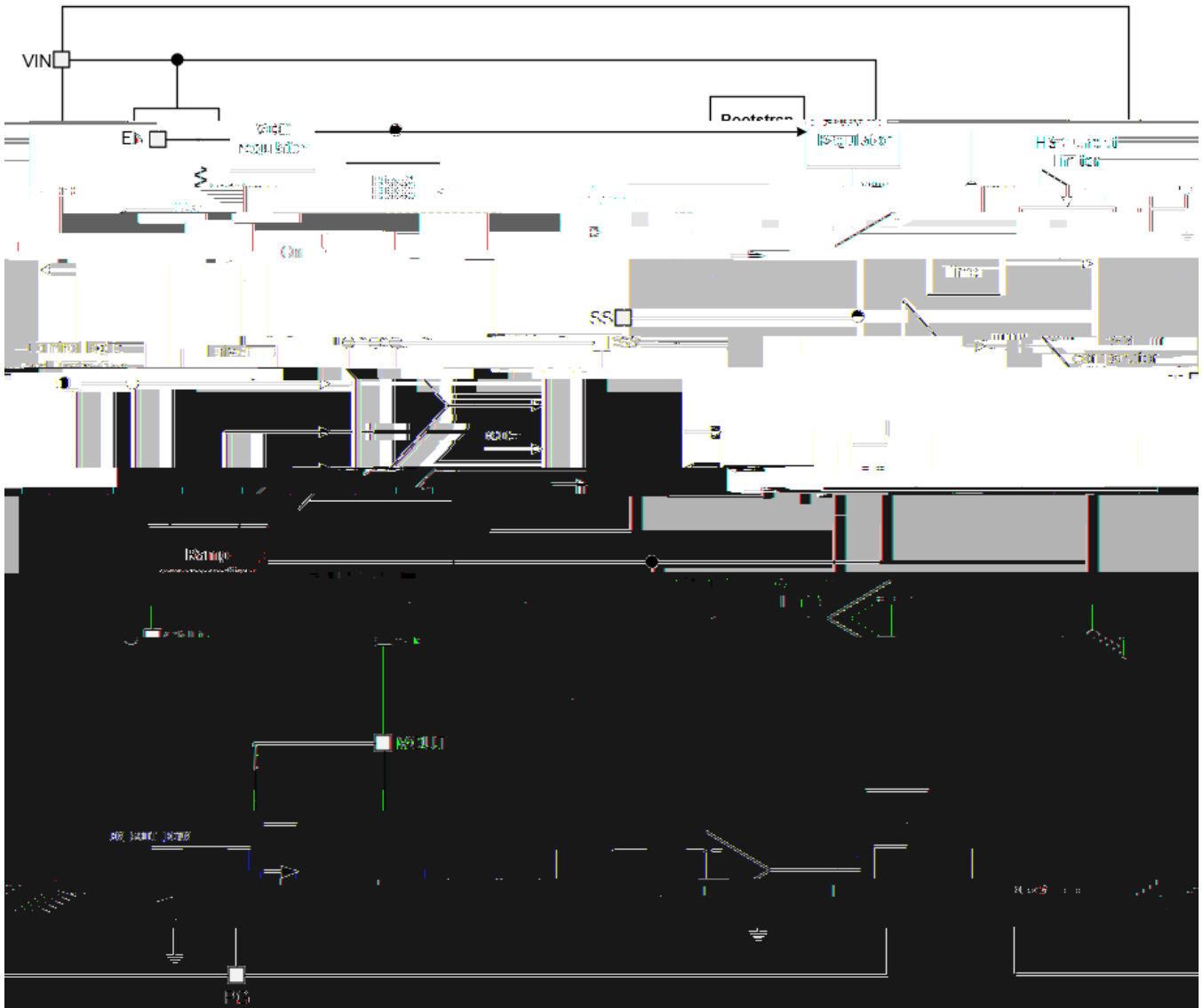


Figure 7. Functional Block Diagram

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When the device is disabled, the part automatically goes into output discharge mode, and its internal discharge MOSFET in VOUT pin provides a discharge path for the output capacitor.

Output Voltage

The SCT2132Q regulates the internal reference voltage at 0.6V. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 2 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$\text{---} \tag{2}$$

Where:

R_{FB_TOP} is the resistor connecting the output to the FB pin.

R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Soft Start (SS)

The SCT2132Q has an external soft start (SS) pin that ramps up the output voltage at a controlled slew rate to avoid overshoot at startup. The SS pin's charge current is typically 3 μ A. The soft-start time (tss) is determined by the SS capacitor. tss can be calculated with Equation 3:

$$\text{---} \tag{3}$$

Where:

C_{SS} is the external SS capacitor.

I_{SS} is the internal 3 μ A SS charge current.

The minimum SS capacitor is recommended to be 1nF.

Over Current Protection (OCP) and Hiccup Mode

In each switching cycle, the inductor current is sensed by monitoring the high-side MOSFET during the ON period and the low-side MOSFET during the OFF period. When the inductor current (IL) reaches the high-side MOSFET peak current limit (typically 4.5A) during the ON period, the high-side MOSFET is forced off immediately to prevent the current from rising further. Then the low-side MOSFET turns on and stays on until IL drops below the low-side MOSFET valley current limit (typically 3.5A). If output loading continues to increase, output will drop below the V_{UVP} , and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup waiting time and restart normally after 7 cycles' soft-start period. If overload or hard short condition still exists during soft-start and make FB voltage lower than V_{UVP} , the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

Power Good Indicator

The SCT2132Q has one power good (PG) output to indicate normal operation after the soft-start time. PG is the open drain of an internal MOSFET, which has a maximum RDS(ON) below 200 . PG can be connected to VIN or an external voltage source through an external a resistor (e.g., 100k). After the input voltage is applied, the MOSFET turns on, and PG is pulled to GND before soft start is ready. After V_{FB} reaches 95% of V_{REF} , PG is pulled high by the external voltage source with 80us delay. When V_{FB} drops to 90% or rises to 110% of V_{REF} , the PG

voltage is pulled to GND to indicate an output failure. If VIN and EN are not available, and PG is pulled up by an external power supply, PG will self-bias and assert. If a 100k pull-up resistor is used, the voltage on the pin is below 0.4V.

Thermal Shutdown

Once the junction temperature in the SCT2132Q exceeds 160 °C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 140 °C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 10.2K . Use Equation 4 to calculate R1.

$$\text{---} \quad (4)$$

where:

V_{REF} is the feedback reference voltage, typical
0.6V

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 12 desired.

$$\text{-----} \tag{12}$$

Where:

- is the output voltage ripple.
- f_{sw} is the switching frequency.
- L is the inductance of inductor.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 10µF ceramic output capacitors work for most applications.

Table 2: Component List with Typical Output Voltage BOM list

| | | | | | |
|--|--|--|---|---|--------|
| | | | | | |
| | | | K | K | option |
| | | | K | K | option |
| | | | K | K | 22pF |

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Application Waveforms

$V_{IN}=5V$, $V_{OUT}=1.2V$, unless otherwise noted

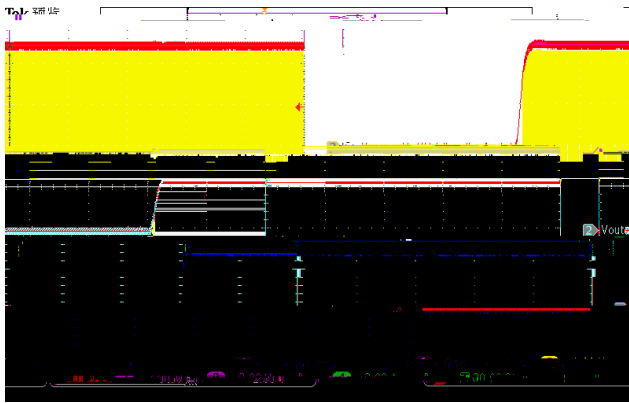


Figure 9. Power up ($I_{LOAD}=3A$)

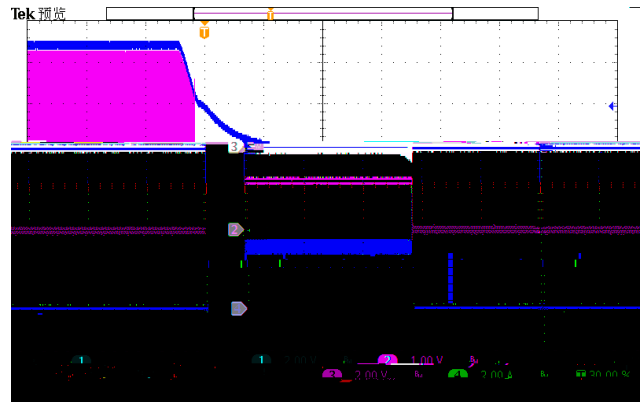


Figure 10. Power down ($I_{LOAD}=3A$)

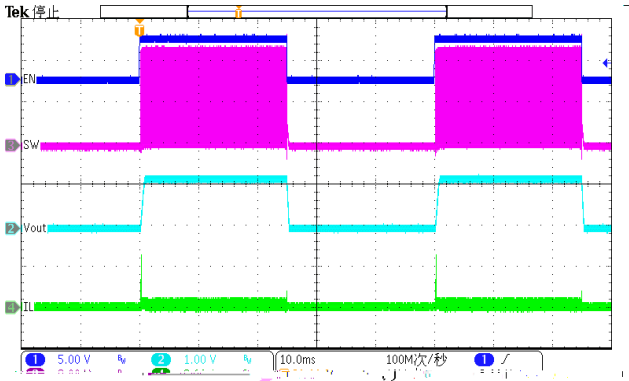


Figure 11. EN toggle ($I_{LOAD}=0.1A$)

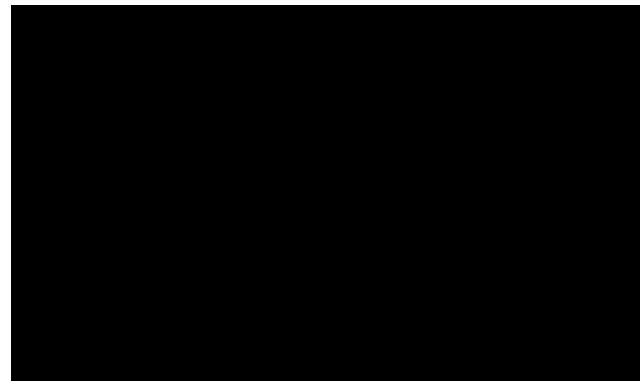


Figure 12. EN toggle ($I_{LOAD}=3A$)

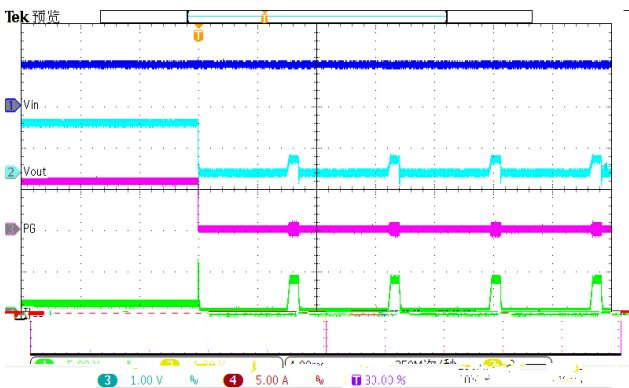


Figure 13. Over Current Protection (1A to hard short)

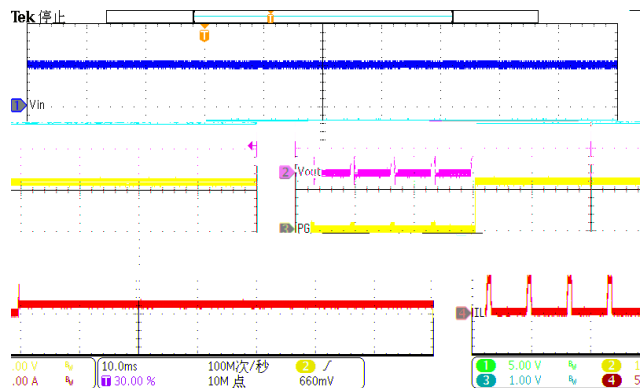
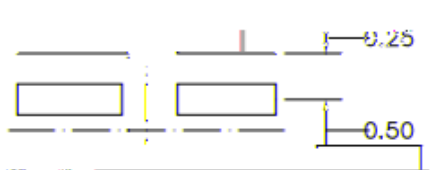
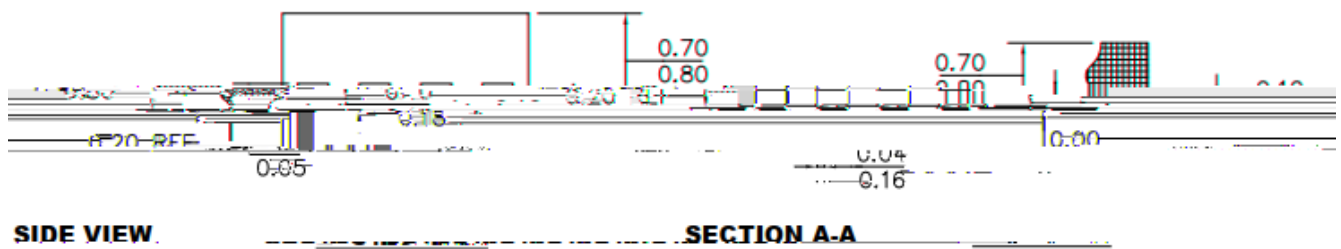
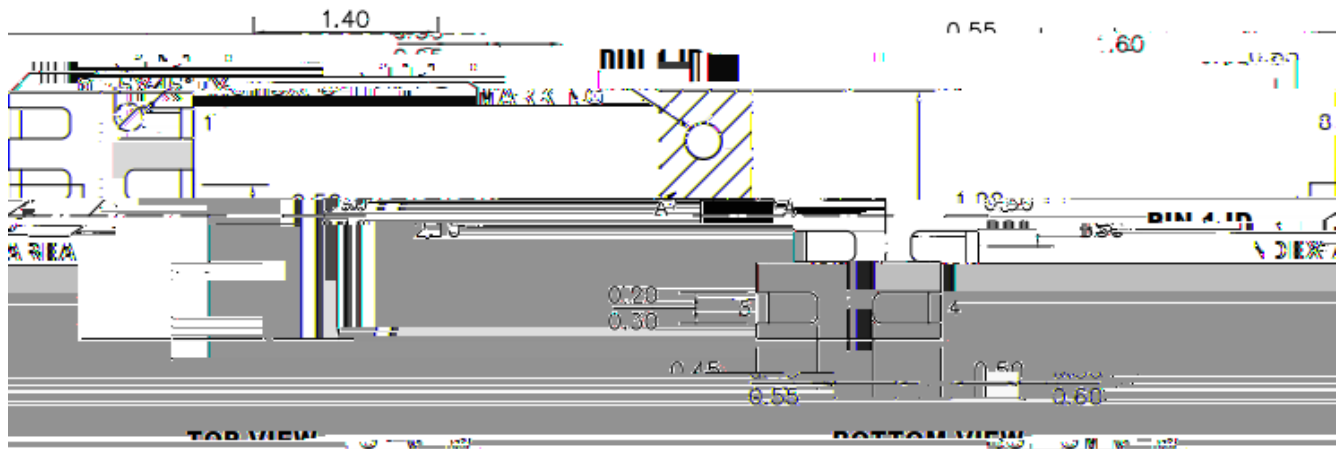


Figure 14. Over Current Release (hard short to 1A)

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NOTE:

1) THE LEAD SIDE IS WETTABLE.

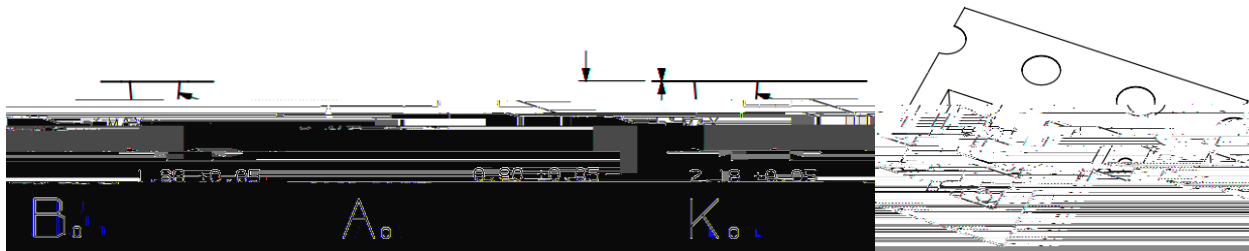
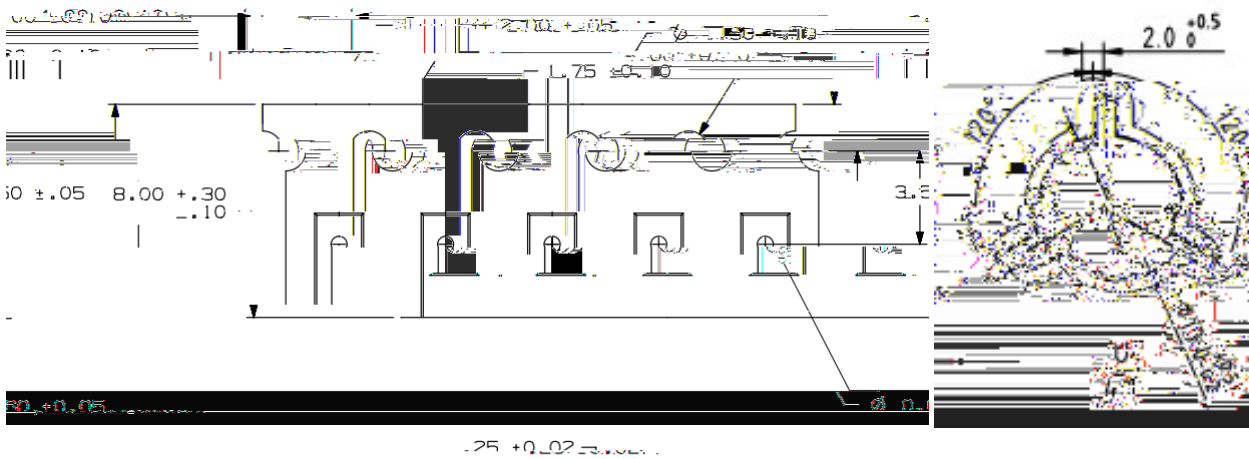
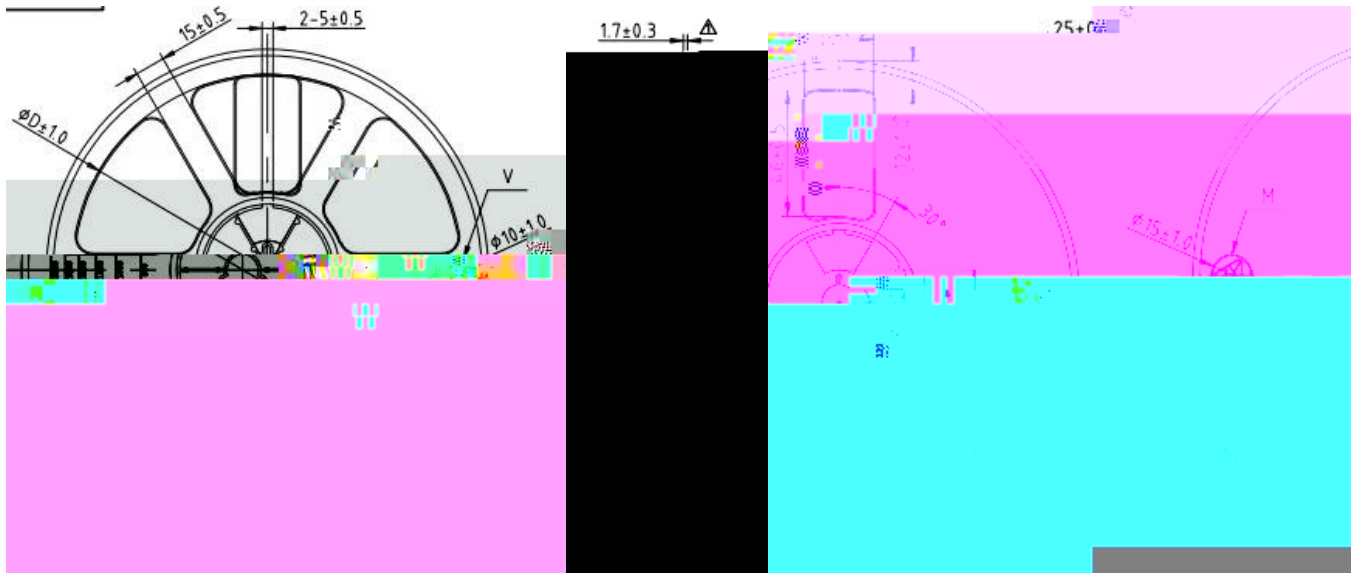
- 2) THE LEAD SIDE IS WETTABLE.
- 3) THE LEAD SIDE IS WETTABLE.
- 4) JEDEC REF.
- 5) DRAWING IS NOT TO SCALE.

1.05 0.20 0.15 0.25 1.05

DAI 4/20/2024

RECOMMENDED LAND PATTERN

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